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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/787,437

02/27/2004

Naoki Yamamoto

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04/05/2005

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EXAMINER

SOWARD, IDA M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/787,437

Applicant(s)

YAMAMOTO, NAOKI

Examiner

Ida M. Soward

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☒ Claim(s) 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/639,306.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2-27-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the application filed March 11, 2004.

Priority

Applicant is reminded that in order for a patent issuing on the instant application to obtain the benefit of priority based on priority papers filed in parent Application No. 09/639,306 under 35 U.S.C. 119(a)-(d) or (f), a claim for such foreign priority must be timely made in this application. To satisfy the requirement of 37 CFR 1.55(a)(2) for a certified copy of the foreign application, applicant may simply identify the application containing the certified copy.

Information Disclosure Statement

The information disclosure statement filed February 27, 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

The disclosure is objected to because of the following informalities: "CO" should have been Co on page 14, line 18.

Appropriate correction is required.

Claim Objections

Claim 7 is objected to because of the following informalities:

1. “**date**” should have been **gate** in lines 4 and 11; and
2. “**poly**” should have been **poly-** in line 12.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not understood which MOS transistor contains the single impurity and which contains both the n-type and p-type impurities.

Line 6 states the polycrystalline silicon film of the NMOS contains the single p-type impurity. Lines 7-8 state polycrystalline silicon film of the PMOS contains the n-type and p-type impurities. Lines 9-13 state the n-type and p-type impurities are contained in the polycrystalline silicon of the NMOS.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mogami (5,656,519) in view of Yang (US 6,468,872 B1).

In regard to claims 1 and 7, Mogami teaches a semiconductor device having an NMOS and a PMOS, comprising:

each gate electrode of the NMOS and PMOS containing a polycrystalline silicon film 6 formed on a gate insulating film 5 and a metallic nitride 31 film formed on the polycrystalline silicon film 6 (Figure 9G, columns 7-8, lines 45-50 and 1-4, respectively).

In regard to claim 7, Mogami teaches a metallic film 33 formed on the metallic nitride film 31 (Figure 9G, column 8, lines 1-4).

As best understood however, Mogami fails to teach a gate electrode of the PMOS containing a p-type impurity and a gate electrode of the NMOS containing a p-type impurity and an n-type impurity.

Yang teaches a gate electrode of the PMOS 73-1 containing a p-type impurity and a gate electrode 73-2 of the NMOS containing a p-type impurity and an n-type impurity (Figures 7B-7C, column 5, lines 19-48).

In regard to limitation concerning an n-type impurity segregated to a side of an interface of the polycrystalline silicon film and a gate insulating film, and a p-type impurity segregated to a side of an interface of a metallic nitride film and the polycrystalline silicon film, the semiconductor device structure as taught by Mogami and Yang is capable of having its impurities segregate to the interfaces claimed. The patentability of an apparatus is determined by its structure not how it functions. Moreover, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the CMOS semiconductor device structure as taught by Mogami with the CMOS semiconductor device having a gate electrode of the PMOS containing a p-type impurity; and a gate electrode of the NMOS containing a p-type impurity and an n-type impurity as taught by Yang to provide a simplified method of fabricating a CMOS semiconductor device by counter-doping using a single impurity doping mask (column 2, lines 22-24).

In regard to claim 2, Mogami teaches each gate electrode of the NMOS and PMOS contains a metallic film 33 formed on the metallic nitride film 31 (Figure 9G, column 8, lines 1-4).

In regard to claims 3-4 and 8, Mogami teaches the p-type impurity being boron and the n-type impurity being phosphorus (Figure 3A, column 5, lines 1-18).

Claims 5-6 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mogami (5,656,519) and Yang (US 6,468,872 B1) as applied to claims 1-4 and 7-8 above, and further in view of Wristers et al. (5,674,788).

Mogami and Yang teach all mentioned in the rejection above. However, Mogami and Yang fail to teach a gate insulating film of silicon oxynitride.

Wristers et al. teach a gate insulating 28 film of silicon oxynitride (Figures 7-8, columns 6 and 8, lines 64-65 and 11-17, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the CMOS semiconductor device structure as taught by Mogami and the CMOS semiconductor device having a gate electrode of the PMOS containing a p-type impurity; and a gate electrode of the NMOS containing a p-type impurity and an n-type impurity as taught by Yang with the MOS semiconductor device having a gate insulating film of silicon oxynitride as taught by Wristers et al. to control boron diffusion and hot electron trapping (column 7, lines 1-25).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to CMOS semiconductor devices:

Bergonzoni (4,968,639)	Bronner et al. (6,087,225)
Davies et al. (4,420,344)	Kang et al. (5,278,441)
Liang et al. (6,355,962 B1)	Nagabushnam et al. (5,888,588)
Tsui et al. (5,960,289)	Wristers et al. (5,674,788).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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IMS
March 31, 2005

Atty M. Sawant
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